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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,766	10/29/2003	Akira Yamanoue	032069	5286

38834 7590 06/29/2006

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,766	YAMANOUE ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-17-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04-17-06 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 2, 4, 5, 9 and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by Sugiyama et al. (US Pat. 2002/0040986)

Regarding claims 1, 2, 4, 5, 9 and 10, Sugiyama et al. disclose a semiconductor device comprising:

- a first insulating/dielectric film/layer/FIL (see 88 in Fig. 7; section 0057) formed over semiconductor substrate (80 in Fig. 7)
- a second insulating/dielectric film/layer/SIL (see 90 in Fig. 7F) formed over the FIL
- an interconnection structure buried the FIL and SIL (see 100/104 in Fig. 7; section 0057), the interconnection structure being in a form of contact holes and pads (see 104/100 in Fig. 7)
- a first dummy pattern of a first conducting layer (see 102 in Fig. 7; section 0058) buried in at least a surface side of the FIL near the interconnection structure
- a second dummy pattern formed of a second conducting layer (see 102 in Fig. 7; section 0058) buried the SIL near interconnection structure and connected to the first dummy pattern through a via/plug portion (see 106 in Fig. 7), the via portion connected to the first dummy pattern being formed in a part of the discrete patterns (see Fig. 6 and 7)
- the interconnection structure further including a first interconnection pattern (see 100 in the FIL in Fig. 7) formed of the first conductive layer in the FIL and a second interconnection pattern (see 100 in the SIL in Fig. 7; section 0057) formed of the second conductive layer buried in the SCIL and connected to the first interconnection pattern through a via/plug/groove-shaped portion/pattern (see 104 in Fig. 7), and

- the first and the second dummy patterns comprising a plurality of discrete patterns which are adjacent to each other and disposed in a multiple numbers/rows periodically at even intervals (see 74 in Fig. 6; sections 0016, 0034 and 0059) so as to make a pattern density of the first, second and the top conducting layers substantially uniform in respective planes

(Fig. 6 and 7; sections 0054-0073; pp. 1-5).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (US Pat. 2002/0040986) in view of Hasegawa et al. (US Pat. 6452274).

Regarding claim 6, Sugiyama et al. teach substantially the entire claimed structure as applied to claim 1 above, except the first conducting layer and the second conducting layer being formed of a conducting material mainly based on copper.

Hasegawa et al. disclose a device (Fig. 7F) having an interconnection structure wherein the interconnection structure comprises a first/second interconnection pattern

having first/second conducting layer respectively formed of conventional copper (71/81 in Fig. 7F; Col. 21, line 15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first conducting layer and the second conducting layer being formed of a conducting material mainly based on copper as taught by Hasegawa et al. so that the desired electrical performance/characteristics can be achieved in Sugiyama et al's device.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (US Pat. 2002/0040986) in view of Matsunaga et al. (US Pat. 6559548).

Regarding claim 7, Sugiyama et al. teach substantially the entire claimed structure as applied to claim 1 above, except the FIL and the SIL being formed of films based mainly on different insulating materials with each other.

Matsunaga et al. teach a conventional interconnect structure (see Fig. 7E) comprising insulating film and conductive wiring/pattern having vias and plugs (see 74/76/75 in Fig. 7E) wherein Matsunaga et al. further teach using various insulating films being made of different material including a phospho-silicate glass, organosilicate glass (OSG), silicon oxide, etc. to achieve the desired dielectric properties and modulus (see 71, 74, 80, etc. in Fig. 7E; Col. 8, line 55- Col. 9, line 16).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the FIL and the SIL being formed of films based mainly on different insulating materials with each other as taught by Matsunaga et al. so that the desired dielectric/insulation and etch properties can be achieved in Sugiyama et al's device.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (US Pat. 2002/0040986) and Matsunaga et al. (US Pat. 6559548) as applied to claims 1 and 7 above, and further in view of Shaffer, II et al. (US Pat. 2002/0052125).

Regarding claim 8, Sugiyama et al. and Matsunaga et al. teach substantially the entire claimed structure as applied to claims 1 and 7 above, except the first and the second insulating film being mainly formed of a polyallyl ether resin and organosilicate glass (OSG) respectively.

Shaffer, II et al. teach using an organic dielectric insulating material in an interconnect structure where the organic material comprises a number of polymers including an organosilicate resin and polyarylene ether resin wherein functional /substitutional groups include a variety of groups including alkyl, alkenyl, alkylene, allyl, aryl alkoxy, etc. to achieve the desired dielectric properties, adhesion and etching characteristics (see sections 0037-0042).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first and the second insulating film being mainly formed of a polyallyl ether resin and organosilicate glass (OSG) respectively as taught by Shaffer, II et al. so that the desired dielectric properties, adhesion and etching characteristics can be achieved in Matsunaga et al. and Sugiyama et al's device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

6-20-05

NITIN PAREKH

PRIMARY EXAMINER

Technology Center 2800